INDUCTOR CURRENT SENSING SCHEME FOR PWM REGULATOR

CROSS-REFERENCE TO RELATED APPLICATION

[001] The present application claims the benefit of previously filed, co-pending Application Serial No. 60/545,367, filed February 18, 2004, by K. Xing, entitled: "An Inductor Current Sensing Scheme for PWM Regulators," assigned to the assignee of the present application and the disclosure of which is incorporated herein.

FIELD OF THE INVENTION

[002] The present invention relates to DC-DC converters and is particularly directed to a new and improved circuit architecture for sensing current in the output inductor coupled to an output load of a pulse width modulator (PWM) driven DC-DC converter.

BACKGROUND OF THE INVENTION

[003] Figure 1 is a reduced complexity illustration of a typical buck mode DC-DC converter, having an upper switch SWU and a lower switch SWL, each of which is

customarily implemented as a field effect transistor, coupled in series between a source of input voltage Vin and a reference terminal (e.g., ground). An inductor is coupled between the common node 10 between the two switches (node 10 often referred to as the phase node) and an output node 20 to which a capacitor C is coupled. In the schematic illustration of Figure 1, the inductor has been shown as a parasitic resistor DCR (direct current resistance) in series with an inductor L. Respective upper gate drive and lower gate drive signals are applied to the gates of the MOSFETs of which the upper and lower switches SWU and SWL are respectively configured, so that the switches are turned on and off in a complementary manner.

[004] In order to achieve certain control related to inductor or load current and provide over-current protection for the converter, current information is required. This has been traditionally obtained by sensing the voltage or current of the components connected to the phase node, such as the lower switch, the upper switch and the inductor. On conventional implementation for this purpose is diagrammatically illustrated in Figure 2, which has series-coupled resistor Rs and capacitor Cs connected in parallel with the inductor L. The R and C construct a low pass filter which will filter out the ac voltage. And the voltage across the capacitor will reflect the current information through the inductor L. Namely, this voltage can be used to measure inductor current. Typically,

however, the value of this voltage is only in the millivolt range as the DCR is generally measured in milliohm range.

SUMMARY OF THE INVENTION

[005] In accordance with the present invention, there is provided a new and improved measurement circuit for sensing the current through the output inductor of a PWM regulator, in a manner that enjoys a considerably improved signal-to-noise ratio compared with the conventional sensing scheme described above. To this end the invention incorporates as part of the PWM controller for the converter, a current generator that is operative to generate a sense current Isense, that is a function of the phase node voltage and the output voltage, in particular, a function of the difference between the phase node voltage and the output voltage, so that Isense =K(Vphase - Vout) in which K is a constant. This sense current Isense is then applied via an Isen port to a parallel resistor-capacitor network Rs and Cs coupled to ground. With the precursor requirement that Rs*Cs = L/DCR, the voltage across Rs and Cs is representative of inductor current. This voltage can be shifted up or down as desired to provide offsets in various applications as required.

[006] A principal benefit of the inductor measurement circuit of the invention is the fact that it uses large magnitude signals, such as phase node and output voltage signals, to generate current information in a sensing

circuit separated from the power converter, so that it has a very high signal-to-noise ratio. The voltage on the sensing circuit is referenced to the operational ground of the IC, so that it enjoys good noise immunity. In addition, it employs the parasitic resistance of the inductor and does not generate additional power loss, so that it offers the convenience for control and over current protection of the PWM regulator. It should also be noted that this circuit can be used for other types of PWM regulator, such as, but not limited to, boost and buck-boost type regulators.

BRIEF DESCRIPTION OF THE DRAWINGS

[007] Figure 1 is a reduced complexity illustration of a typical buck mode DC-DC converter;

[008] Figure 2 shows a conventional implementation of a circuit having series-coupled resistor Rs and capacitor Cs connected in parallel with the inductor L of the circuit of Figure 1, for deriving load current information;

[009] Figure 3 diagrammatically illustrates an equivalent circuit around the inductor branch represented as a pair of voltages applied to its end terminals;

[010] Figure 4 is an associated dual circuit of the network of Figure 3, having current sources I1 and I2 proportional to the voltages V1 and V2, respectively, with the time constant of the components Rs and Cs being matched with that of the inductor branch; and

[011] Figure 5 shows the application of the circuit of Figure 4 to an integrated circuit (IC) PWM controller.

DETAILED DESCRIPTION

[012] Attention is now directed to Figure 3, which diagrammatically illustrates an equivalent circuit around the inductor branch being represented as a pair of voltages applied to its end terminals. In this circuit diagram V1 represents the phase node voltage as a square wave produced by the upper and lower switches SWU and SWL, while V2 is the output voltage. An associated dual circuit of this network may be represented as shown in Figure 4, where the current sources I1 and I2 are proportional to the voltages V1 and V2, respectively, with the time constant of the components Rs and Cs being matched with that of the inductor branch.

[013] Figure 5 shows the application of the circuit of Figure 4 to an integrated circuit (IC) PWM controller 50. In this circuit, the phase node voltage and the output voltage are sensed by the controller IC 50, which generates a sense current Isense that is proportional to the difference between the phase node voltage Vphase and the output voltage Vout. This sense current is then applied via an Isen port to a parallel resistor-capacitor network Rs and Cs coupled to ground. With the precursor requirement that Rs*Cs = L/DCR, the voltage across Rs and Cs is representative of inductor current.

This voltage can be shifted up or down as desired to provide offsets in various applications as required.

[014] A principal benefit of the circuit of Figure 5 is the fact that it uses large magnitude signals, such as phase node and output voltage signals, to generate current information in a sensing circuit separated from the power converter, so that it has a very high signal-to-noise ratio. The voltage on the sensing circuit is referenced to the operational ground of the IC, so that it enjoys good noise immunity. Further, as pointed out above, it employs the parasitic resistance of the inductor and does not generate additional power loss, so that it offers the convenience for control and over current protection of the PWM regulator. It should also be noted that this circuit can be used for other types of PWM regulator, such as, but not limited to, boost and buck-boost type regulators.

[015] While I have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art. I therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.